XLM72 Universal Logic Module

FEATURES

Universal logic module XLM72 is a user-programmable VME (6-U) slave module with high degree of flexibility. It features:

- 72 programmable front-panel ECL ports, configurable in quartets as either inputs or outputs, organized in three 34-pin connectors and one 8-pin connectors. Four ports can be used as external clock ports, supporting rates of up to 110 MHz.
- One user-programmable Field Programmable Gate Array (FPGA), XCS40XL by Xilinx, clocked at 80 MHz.
- One user-programmable, 900-MFlops/s floating-point Digital Signal Processor (DSP), TMS320C6711 by Texas Instruments.
- 2 banks of 2 Mbytes/each of fast Asynchronous Static Random Access Memory (ASRAM), independently accessible by the FPGA, DSP, and VMEBus.
- A custom, programmable, reconfigurable VME Interface and Bus Router/Arbitrator (IBRA), implemented in 4 Complex Programmable Logic Devices (CPLD).
- Supports 16- and 32-bit data transfers and 32-bit block transfers at rates of up-to 40 Mbytes/s.
- One 2-Mbyte Programmable Erasable Read-Only Memory (flash memory) holding up to 4 FPGA configuration files.
- Four front-panel LEDs, one indicating the VME activity, and the remaining three user-programmable.

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The FPGA

The logical operations of XLM72 are programmed by user into an XCS40XL Field Programmable Gate Array by Xilinx. The FPGA features:

- 1862 logic cells
- 40000 system gates
- 784 complex logic cells
- 2012 flip-flops
- 250888 total distributed RAM bits

The FPGA can be configured either from the first bank of ASRAM or from one of the four sectors of the flash memory. Sectors of flash memory can be programmed individually using a utility configuration of FPGA.

Possible Applications

- FERA receiver/memory
- Complex trigger logics, including digital gate and delay generators.
- Scalers, prescalers, coincidence registers.
- Time stamping.
- Readout of various detector systems.
- Intelligent data buffer

Due to the parallel nature of the FPGA, XLM72 can run various applications concurrently, limited only by the size of the FPGA resources. For example, one part of XLM72 resources can be used to implement an intelligent FERA receiver/memory, while other part as trigger logics, and yet another part as a time stamper or a set of gated and non-gated scalers and coincidence registers.

Requires

VME crate with CERN extension, i.e., with a 30-pin JAUX middle connector supplying –5.2V and –2V ECL power, as well as the geographic addressing.

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